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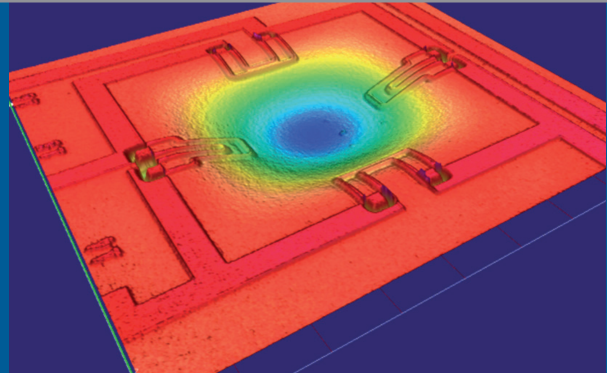


1 *MEMS for high temperature: SOI-technology and high temperature metallization allow operation exceeding 250 °C*
2 *3D-view of membrane of a piezoresistive pressure sensor*
3 *Trench isolated SOI (Silicon on insulator) device*
4 *Hall-sensor element realized in HT-CMOS technology*

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

Finkenstr. 61
D - 47057 Duisburg
Phone +49 203 37 83-0
Fax +49 203 37 83-266
www.ims.fraunhofer.de

Contact
Michael Bollerott
Phone +49 203 37 83-227
vertrieb@ims.fraunhofer.de

MEMS FOR HARSH ENVIRONMENTS

Generic technology for robust MEMS

Optical MEMS for harsh environments are typically needed for specific application fields such as oil exploration, chemical industry and the aerospace or automotive sector.

In many cases the sensing device has to be placed in close contact to the system to be measured and thus is exposed, for example, to high temperatures and/or aggressive chemicals and media.

Many silicon based sensors typically rely on piezoresistive doped resistors in a silicon substrate. For temperatures exceeding 125 °C bulk silicon based devices with pn-junction isolation cannot be used anymore since thermally induced leakage currents limit the device performance. This restriction can be overcome by dielectric isolation. Moreover, conventional aluminum metallization strongly degrades by electromigration effects when operated under high temperature condition, thus limiting long term stability and reliability. Thus special metallization is required.

In some cases the direct contact of the sensing element with the surrounding aggressive medium is unavoidable, e.g. in order to optimize response times.

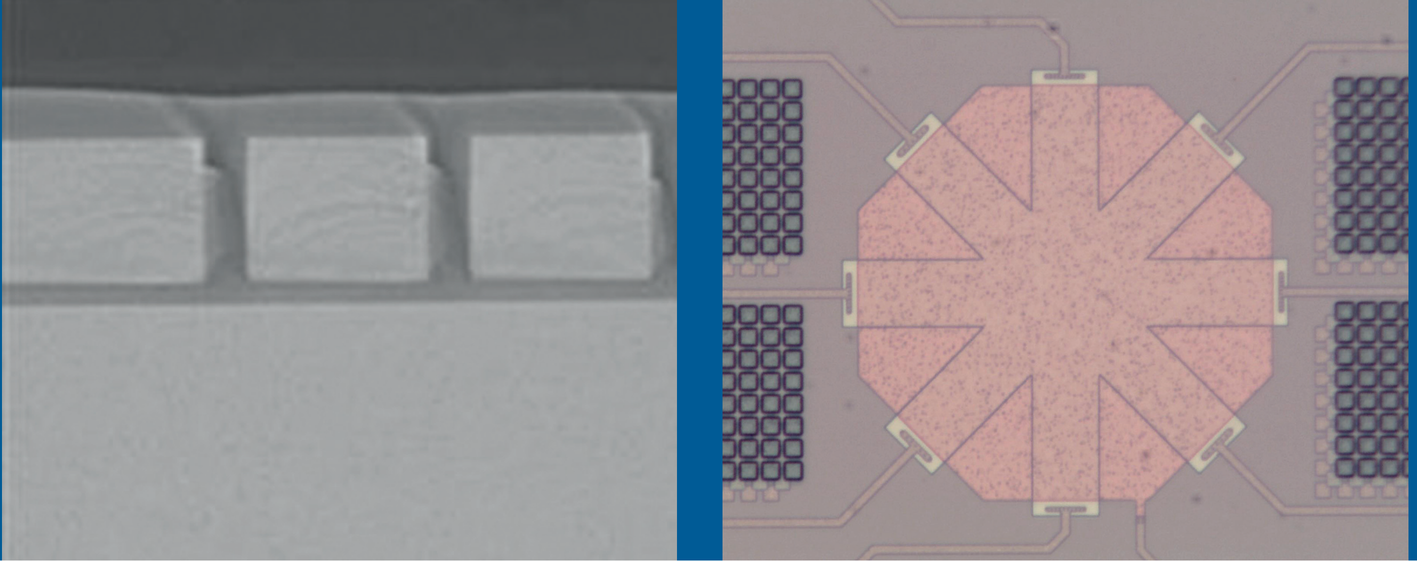
The combination of chemically aggressive media and high temperature implies especially high demands on device passivation in order to avoid degradation of the sensing element. For adequate protection layers based on ALD have been developed.

Silicon on Insulator based Technology

A silicon-on-insulator (SOI) based technology with trench isolation can be used for high temperature applications exceeding 250 °C. Since crystalline silicon exhibits besides its excellent electronic also superior mechanical and piezo-resistive properties, the silicon film of an SOI-wafer is ideally suited for MEMS devices such as pressure sensors, acceleration sensors, microphones etc.

Employing bulk micromachining technologies like deep reactive ion etching the silicon film can be used for membrane and cantilever structures.

The combination of the favorable piezore-



sistive coefficient of silicon with dielectric trench isolation enables high performance piezoresistive resistors for HT applications.
For long-term stability in high temperature environments a tungsten metallization is used, which is also employed in existing HT-CMOS-processes. On top of the tungsten pad an aluminum layer or a Cu-Ni-Au bump can be deposited in order to provide an interface for wire bonding.

Combination with HT-CMOS

Due to timing restrictions or for improved noise immunity in many applications microelectronic circuitry is placed close to the sensor element, for example for

- Signal amplification or conversion (ADC)
- Data transmission (wire/wireless)
- Control and regulation functions.

To support the full advantage of HT-MEMS a corresponding CMOS technology is available with the same harsh environment and high temperature capabilities as the HT-MEMS sensors.
In order to limit leakage currents it is also based on thin film SOI wafers.
For MEMS-CMOS integration Flip-Chip bonding by HT-SLID-technology is available. The SLID technology enables high temperature resistant electrical bump contacts that mechanically and electrically connect MEMS and read out chip.

Key features of HT CMOS technology

IMS offers a thin film SOI-technology for high temperature applications.
The core properties are listed below

- 0.35 µm design rules
- Operation temperature >250 °C (depends on performance requirements)
- Analog grade devices
- 3.3 V core
- Gate count: 8,500 gates/mm²
- Supply voltage analog and IO: 10V
- Dual gate oxides
- 4 layers tungsten metallization
- EEPROM, analog C, TOX-based OTP
- Integrated Hall-sensor under develop.

Process access:

- CADENCE design kit
- Multi-project wafers

As a special feature Hall-plates can be realized within the CMOS-process for magnetic sensing at high temperature.
A microscopic view of a Hall-sensor element is shown in Figure 4.

IMS realizes your individual sensor concept – from first idea to pilot production

Based on the existing SOI technologies IMS can provide customized MEMS-solutions for high temperature and harsh environment.

With the aid of FEM based simulation we can support the concept and design phase and conduct the development in a professional cleanroom environment according to our quality assurance.

Please contact us for discussing your request.

Technological parameters HT-MEMS

Wafer size:	200 mm
Technology:	Silicon on insulator with dielectric isolation
Film thickness:	1-4 µm
Metallization:	Tungsten
Pad metallization:	Aluminum or Cu-Ni-Au-bumping
Trench isolation:	Oxide
Piezoresistors:	Typically 2-5 kΩ
Backside processes:	DRIE and wafer bonding
Alignment accuracy (frontside to backside):	<1 µm
Optional additional media resistant passivation:	ALD
Combination with 0.35 µm HT-CMOS possible. Interconnection technology:	SLID-bonding